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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,415	01/03/2006	Kees Marinus Maria Van Kaam	NL03 0806 US1	4525

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NXP, B.V.  
NXP INTELLECTUAL PROPERTY DEPARTMENT  
M/S41-SJ  
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SAN JOSE, CA 95131

EXAMINER
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KERVEROS, JAMES C

ART UNIT	PAPER NUMBER
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2117

NOTIFICATION DATE	DELIVERY MODE
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04/08/2008

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

## Office Action Summary

**Application No.**

10/563,415

**Applicant(s)**VAN KAAM, KEES MARINUS  
MARIA**Examiner**

JAMES C. KERVEROS

**Art Unit**

2117

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☒ Claim(s) 1-24 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 January 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This is a non-Final Office Action in response to the present US Application 10/563415, filed 01/03/2006.

Claims 1-24 are presently under examination and pending.

### ***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file, for EUROPEAN PATENT OFFICE (EPO) Application No. 03102062.1, filed 07/09/2003.

The U.S. Application No. 10,563415, filed 01/03/2006, is a national stage entry of PCT/IB04/51089, International Filing Date: 07/01/2004.

### ***Drawings***

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because the "voltage controller" and "clock controller" described in the specification are designated as "Controlled voltage" and "Controlled frequency" with the corresponding reference characters in Figs. 2-4. The drawings should be changed accordingly to be consistent with the description in the specification.

Also, Fig. 1 should be deleted, or corrected accordingly, since there is no Shmoo plot information for the device under test.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

Claims 1-24 are objected to because of the following informalities:

Claims 1, 23, the transitional phrase "characterized by" should be changed to "wherein", for consistency with the rest of the claimed language.

The term "operable", as recited in passim in the claims, should removed from the claims, because "operable" implies that the unit or the device may not operate always.

Also the terms "characterization" unit or "characterization" data should be changed to "test" unit or "test" data, to comply to US practice, since in this case the term "characterization" means "test".

The claims are generally failing to conform to current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 4-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hartnett (US Patent No. 6,427,217) issued July 30, 2002.

Regarding independent Claims 1, 20, 23, Hartnett discloses a semiconductor device (integrated circuit 200) comprising an IEEE 1149 TAP controller 231, such as an integral characterization unit, for providing test data to a functional device (logic under test 201).

Regarding Claims 2, 4, 7, 8, 10-12, 19, 21, 24, Hartnett discloses IEEE tap controller 231 provides the EXTEST and TEST\_EN signals over connections 238 and 239 respectively. These signals will be used to control the operation of multiplexers 216 and 218, respectively. IEEE tap controller 231 also provides over connection 234 a group of control signals to clock controller 232, which supplies the functional clocks over connection 236 and the boundary clocks over connection 237. In block 87, Figs. 3, the clock controller 232 issues at least two clocks pulses to the device. In this manner, the logic under test 201 receives clock input signals such that an operational state is simulated.

Regarding Claims 5, 6, 9, 13-19, 22, Hartnett discloses (logic under test 201) receives test data (TDI) and produces a test response (TDO) as shown by the flow chart in Fig. 4, illustrating the operation of device test logic 100 with respect to device testing.

Data is loaded into the boundary scan ring 222 over connection 221 and data (TDI) is loaded into functional scan ring 228 over connection 212. The functional registers are clocked in their normal operation and the boundary scan registers are incrementally clocked, or shifted by one bit position. The boundary scan registers 217 are shifted in lock step with the system clock. The information contained in boundary scan registers 217 can be sampled out of the boundary scan ring 222 over connection 226 (TDO).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hartnett (US Patent No. 6,427,217) in view of Schwarz (US Patent No. 6,496,947).

Regarding Claim 3, Hartnett does not disclose a control signal to control a voltage supply of the device. However, in analogous art, Schwarz (US 6496947) discloses a voltage regulator circuit 502, which is controlled by BIST circuit 18, Fig. 7,

Art Unit: 2117

and provides the supply voltage for memory array 12. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a voltage regulator circuit as taught by Schwarz in the device of Hartnett for the purpose of reducing the memory supply voltage during the test pause, as show at step 402 in Fig. 6, thus reducing heat dissipation and power energy.

### ***Pertinent Art***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMES C KERVEROS/  
Primary Examiner, Art Unit 2117

Date: 4 April 2008  
Office Action: Non-Final Rejection

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